IN THE CLAIMS

Please cancel claims 1-16 without prejudice.

Please add claims 17-32 as follows:

~~Patent Claims~~WHAT IS CLAIMED IS:

1-16 (cancelled)

17. (New) A method to assemble a substrate for a semiconductor package comprising:

providing a substrate comprising a sheet of core material and a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and conducting vias connecting the upper conducting traces and lower conducting traces;

forming a plurality of vent holes in the substrate; and

covering the upper and lower surfaces of the substrate by a layer of solder resist leaving the contact areas free from solder resist.

18. (New) The method to assemble a substrate of claim 17, wherein the vent holes are closed at one end by a layer of solder resist on the upper surface of the substrate.

19. (New) The method to assemble a substrate of claim 17, wherein the vent holes include solder resist.

20. (New) The method to assemble a substrate of claim 17, wherein the vent holes are formed by drilling.

21. (New) The method to assemble a substrate of claim 17, further comprising forming the vent holes in the core material before a plurality of upper contact traces and upper contact

pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and depositing conducting vias.

22. (New) A method to assemble a semiconductor package comprising:

providing a substrate comprising a sheet of core material and a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and conducting vias connecting the upper conducting traces and lower conducting traces;

forming a plurality of vent holes in the substrate;

covering the upper and lower surfaces of the substrate by a layer of solder resist leaving the contact areas free from solder resist;

providing a semiconductor chip comprising an active surface including a plurality of chip contact areas;

mounting the chip on the upper surface of the redistribution board by microscopic solder balls between the chip contacts and upper contact areas;

performing a solder reflow; and

underfilling the area between the chip and the upper surface of the redistribution board with epoxy resin.

23. (New) A method to assemble a semiconductor package characterized in that the upper surface of the chip and substrate are covered with mold material.

24. (New) A substrate for a semiconductor package comprising:

a sheet of core material;

a plurality of upper conducting traces and upper contact pads on an upper surface of the sheet, a second plurality of lower conductive traces and external contact areas on a bottom surface of the sheet and a plurality of conducting vias connecting the upper conducting traces and lower conducting traces;

a plurality of vent holes; and

a layer of solder resist covering the upper and lower surfaces of the substrate leaving the contact areas free from solder resist.

25. (New) The substrate of claim 24, wherein the vent holes are include solder resist.

26. (New) The substrate of claim 24, wherein the vent holes are closed at one end by a layer of solder resist on the upper surface of the substrate.

27. (New) The substrate of claim 24, wherein the plurality of vent holes are laterally located towards the center of the substrate.

28. (New) The substrate of claim 24, wherein the plurality of vent holes are laterally located towards the center and towards the outer edges of the substrate.

29. (New) The substrate of claim 24, wherein the vent holes have a diameter of approximately 1μm to approximately 5mm or approximately 10μm to approximately 0.5mm or approximately 100μm.

30. (New) A semiconductor package comprising:

a sheet of core material;

a plurality of upper conducting traces and upper contact pads on an upper surface of the sheet, a second plurality of lower conductive traces and external contact areas on a bottom surface of the sheet and a plurality of conducting vias connecting the upper conducting traces and lower conducting traces;

a plurality of vent holes;

a layer of solder resist covering the upper and lower surfaces of the substrate leaving the contact areas free from solder resist;

a substrate; and

a semiconductor chip including an active surface with a plurality of chip contact areas, electrically connected to the substrate.

31. (New) The semiconductor package of claim 30, wherein the chip is encapsulated by mold material.

32. (New) The semiconductor package of claim 30, wherein the chip is mounted to the substrate by the flip-chip technique.

33. (New) A substrate for a semiconductor package comprising:

a sheet of core material with an upper surface and a bottom surface each covered with a layer of solder resist;

a plurality of upper conducting traces and upper contact pads on the upper surface;

a plurality of bottom conductive traces and external contact areas on the bottom surface;

a plurality of conducting vias connecting the upper conducting traces and bottom conducting traces;

a plurality of vent holes; and

means for leaving the contact areas free from solder resist.

34. (New) The substrate of claim 33, wherein the vent holes include solder resist.

35. (New) The substrate of claim 33, wherein the vent holes are closed at one end by a layer of solder resist on the upper surface of the substrate.

36. (New) The substrate of claim 33, wherein the plurality of vent holes are laterally located towards the center of the substrate.